STATUS OF THE CLAIMS

Claims 1-17 were originally filed in this patent application. In the pending office action, claims 1-17 were rejected under 35 U.S.C. §112, first paragraph. Claims 1-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,301,287 to Herrell *et al.* (hereinafter "Herrell"). No claim was allowed. In this amendment, claims 13-14 have been cancelled, claims 1, 5 and 12 have been amended, and new claims 18-20 have been added. Claims 1-12 and 15-20 are currently pending.

REMARKS

Rejection of claims 1-17 under 35 U.S.C. §112, first paragraph

The examiner rejected claims 1-17 under 35 U.S.C. §112, first paragraph, as allegedly being based on a disclosure which is not enabling. The examiner states that elements critical or essential to the practice of the invention are neither included in the claims nor sufficiently enabled by the disclosure in such a way as to enable one skilled in the art to which it pertains, or most nearly related, to make and/or use the invention.

Applicants respectfully assert that the examiner's rejection under 35 U.S.C. §112, first paragraph, is in error. In essence, the examiner argues that because the prior art teaches virtual addressing schemes, and the claims appear to read on virtual addressing schemes, the disclosure is not enabling. This is an argument that would be more appropriately made under 35 U.S.C. §103(a), not 35 U.S.C. §112, first paragraph. Applicants respectfully assert the examiner has missed the point in his reading of the claims and the specification. The claims and specification clearly recite a memory tag mechanism that is not taught or suggested in the prior art, and use of memory tags that is not taught or suggested in the prior art. The apparatus, method and program product claimed are clearly supported in FIGS. 1 and 6-8 and the corresponding text in the specification. All the pending claims are enabled by the corresponding portions of the specification. Applicants respectfully request reconsideration of the examiner's rejection of claims 1-17 under 35 U.S.C. §112, first paragraph.

Rejection of claims 1-17 under 35 U.S.C. §103(a)

The examiner rejected claims 1-17 under 35 U.S.C. §103(a) as being unpatentable over Herrell. Applicants respectfully assert the examiner's rejection of the claims does not provide a proper mapping of the teachings of Herrell on the limitations in the claims. The examiner provides a detailed explanation of Herrell, but the indication of the relevance of these teachings to the specific language in the claims is provided by a few express mappings and several single-word parentheticals. For example, the only claim language expressly recited in the rejection of claims 1, 5 and 12 is partitions, partition manager, tag, tags, and sizes. Nowhere does the examiner address in the rejection the device driver recited in the claims. Nowhere does the examiner address in the rejection the memory tag that comprises an identifier that does not represent physical memory. Nowhere does the examiner address in the rejection the partition manager that detects when the first address is a memory tag, and if so, returns the second address of the second length that corresponds to the memory tag. For these many reasons, the examiner has failed to establish a prima facie case of obviousness for claims 1-17 under 35 U.S.C. §103(a).

Claims 1, 5 and 12 are amended herein to recite the memory tag comprises an identifier that cannot be mapped to a corresponding location in physical memory, instead of the memory tag comprises an identifier that does not represent physical memory. Applicants' specification at p. 6 line 14 to p. 7 lines 11 discusses in detail the use of the logical memory tag. The memory tags in the specification do not represent physical memory. In the rejection, the examine seems to equate virtual addresses to the memory tags. Virtual addresses do not read on the memory tags in applicants' claims and specification. A virtual address at a high-level could be said to not represent physical memory, because it has to be mapped to a corresponding physical address in physical memory. Claims 1, 5 and 12 are amended herein to recite the memory tag comprises an identifier that cannot be mapped to a corresponding location in physical memory to

distinguish the memory tag in the claims from a logical address. While a virtual address may not directly represent physical memory, it can be mapped to a corresponding location in physical memory. As a result, a virtual address in Herrell does not read on the memory tags recited in claims 1, 5 and 12, as amended.

The memory tags in the claims are a sort of "dummy address" that cannot be mapped to physical memory. This dummy address can be sent to a device driver, which cannot tell the difference between the dummy address and an address that accesses physical memory. When the partition manager receives the memory tag, it detects that it is a memory tag (dummy address), and returns the I/O address corresponding to the memory tag. The result is the ability to perform redirected DMA operations from an I/O adapter in one logical partition to an application in a different logical partition.

Claims 1, 5 and 12 are further amended to recite the partition manager manages allocation of a plurality of hardware resources to a plurality of logical partitions and manages communication between the plurality of logical partitions. This amendment is made to clarify that the invention is in the context of a logically-partitioned computer system, and a memory manager that manages memory partitions in a virtual memory system does not read on the partition manager in the claims as amended.

Claims 13 and 14 have been cancelled, and claim 12 has been amended to incorporate the limitations of claim 13 to comply with the USPTO's current practice in interpreting program product claims under 35 U.S.C. §101 to exclude transmission media.

Applicant respectfully asserts that claims 1, 5 and 12 as amended are allowable over Herrell. Claims 2-4, 6-11, and 15-17 depend on claims 1, 5 and 12, respectively, and are therefore allowable as depending on allowable independent claims.

New claims 18-20

New claims 18-20 have been added herein to recite additional detail regarding a read from an I/O adapter in a first logical partition to a buffer in an application in a second logical partition. Nowhere does Herrell teach or suggest the limitations in claims 18-20. As a result, claims 18-20 are allowable over Herrell or other known prior art.

Conclusion

In summary, none of the cited prior art, either alone or in combination, teach, support, or suggest the unique combination of features in applicants' claims presently on file. Therefore, applicants respectfully assert that all of applicants' claims are allowable. Such allowance at an early date is respectfully requested. The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

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